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ABSTRACT

The performance of arrays consisting of 21 β-Ga_2O_3 field-plated rectifiers fabricated on thick epitaxial layers (n-type carrier concentration $\sim 1.6 \times 10^{16}$ cm^{-3}) grown on conducting substrates (carrier concentration 3×10^{19} cm^{-3}) is reported. We show that by interconnecting the output of 21 smaller (0.4×0.4 mm^2 to 1×1 mm^2, total area 0.09 cm^2) individual rectifiers using e-beam deposited Au, we can achieve a high total forward output current of 33.2 A, at 4.25 V in the single-sweep voltage mode, and a low forward turn-on voltage of 2.9 V (defined at 100 A cm^{-2}) and maintain a reverse breakdown voltage of 240 V (defined at 1 μA cm^{-2}). The current density was 376 A cm^{-2}, and the on-state resistance was 0.012 Ω cm^2. The total forward current was 10 A at 1.9 V and 22 A at 3 V. The power figure-of-merit for the array, V_B^2/R_{ON}, was 4.8 MW cm^{-2}, with a reverse recovery time of individual rectifiers of 32 ns. The on/off ratio of the rectifier array was in the range of 10^5–10^{10} for +1 V/−1 to −100 V.

In recent years, β-Ga_2O_3 has attracted a tremendous amount of attention for its potential in power device applications, due to its ultra-wide bandgap (4.5–4.9 eV) and high critical breakdown field (6–9 MV/cm).[1–9] Wide bandgap semiconductor power switching devices offer improved efficiency and power densities for conversion and control of electrical power during renewable energy generation, utility system energy storage, and electric/hybrid vehicle charging and operation compared to their Si counterparts.[3,10–12] Ga_2O_3 is expected to offer even higher performance than SiC and GaN as well as size reductions in power converters.[3,13–18] There have been recent reports of Ga_2O_3 vertical geometry rectifiers with lower on-state resistance than SiC at the same reverse bias, showing the potential of this material.[19] Indeed, economic analysis of the cost of melt-grown Ga_2O_3 substrates with thick epitaxial layers grown by hydride vapor phase epitaxy indicates that it may be possible to achieve SiC-like performance with nearly Si-like costs.[14,15] The primary limitations of Ga_2O_3 are its low electron mobility and low thermal conductivity.[15,16,20–23] The low electron mobility is caused by the high ionicity of the Ga-O bonds, which gives rise to a factor of three stronger Frölich coupling than for GaN.[16] Although this low electron mobility is intrinsic, the development of $Al_xGa_{1-x}O_3/Ga_2O_3$ heterostructures may provide an avenue for improved mobility with the formation of a two dimensional electron gas (2DEG) channel.[24–26] To alleviate the poor thermal conductivity, epitaxial growth on sapphire has been pursued, which can produce dislocation free growth of the α-polymorph, along with epitaxial liftoff techniques to highly thermally conductive metal supports.[27,28] In addition, β-phase devices may be integrated with diamond or other heat sink materials on both surfaces to improve thermal management, as is done with GaN and SiC.[15,29–34]

For high voltage and high current power device investigations, a vertical device geometry is preferred over lateral device design for the advantage of simultaneous high forward current and current density.[4,6,15] There are many published results in the past demonstrating the high blocking voltage capability for vertical β-Ga_2O_3 rectifiers,[35–43]

including reverse breakdown voltages (V_B) of 2440 V in trench-MOS structures[8] and 2300 V for a 150 μm diameter field-plated planar device (area = 1.77×10^{-4} cm^{-2}).[9] However, demonstrations of very high absolute current β-Ga_2O_3 power devices with reasonable breakdown voltages are limited due to the effect of defect density within the β-Ga_2O_3 drift region. There are reports of 2 A forward current in large area (0.2 cm^2) individual rectifiers.[42] In this work, we report a demonstration of β-Ga_2O_3 field-plated Schottky rectifier arrays with an absolute forward current of more than 30 A in the single sweep mode, while also achieving a reverse blocking voltage of 240 V.

The starting material for device fabrication was a Sn-doped ($n = 3.6 \times 10^{18}$ cm^{-3}) β-Ga_2O_3 single crystal [(001) surface orientation, 650 μm thick, Tamura Corporation, Japan] grown by the edge-defined film-fed technique,[13] with a 20 μm Si doped β-Ga_2O_3 epitaxial layer grown on top of this substrate. The x-ray diffraction full width at half maximum was <150 arc sec for both the substrate and the epi layer. After growth, the epi surface was planarized by chemical mechanical polishing (CMP). The n-drift region was grown by halide vapor phase epitaxy with a carrier concentration of 1.62×10^{16} cm^{-3}, obtained from capacitance-voltage measurements. This gives a range of breakdown voltages from >1 kV for small area devices to 240 V for large devices (0.16–1 mm^2) used for the high current arrays. A higher doping concentration in the drift layer would increase forward current but would decrease reverse breakdown voltage. Cross-sectional transmission electron microscopy showed the epitaxy to be of high quality, with the only defects observed being stacking faults with a density of 1.5×10^{10} cm^{-2}, as shown in Fig. 1. Mahadik *et al.*[44] have reported threading screw dislocation densities of 30 cm^{-2} and basal dislocation densities of 20 cm^{-2} in similar films using synchrotron x-ray to examine an area of ~2 cm^2 and found only ~50 dislocations in the entire chip. TEM is inappropriate for performing this kind of measurement since our field of view is only several microns.[2] Even though we did not see any dislocations, we cannot say, anything other than that the threading dislocation (TD) density is lower than $\sim 10^8$ cm^2. Some of these dislocations propagate from the edge-defined, film-fed growth (EFG) substrate into the halide vapor phase epitaxy layer.[45] Our experimental yield of low leakage current devices is ~50%. In case the extended defects are the origin of high device leakage, the Seeds model for yield (Y) is applicable and given by $Y = 1/(1 + AD)$, where A is the area and D the defect density. Our experimental value then produces a value of D = 100 cm^{-2}, comparable within a factor of two to the total threading screw dislocation and basal dislocation densities. The low defect density and strain in such layers indicate their applicability to device fabrication of practical size.

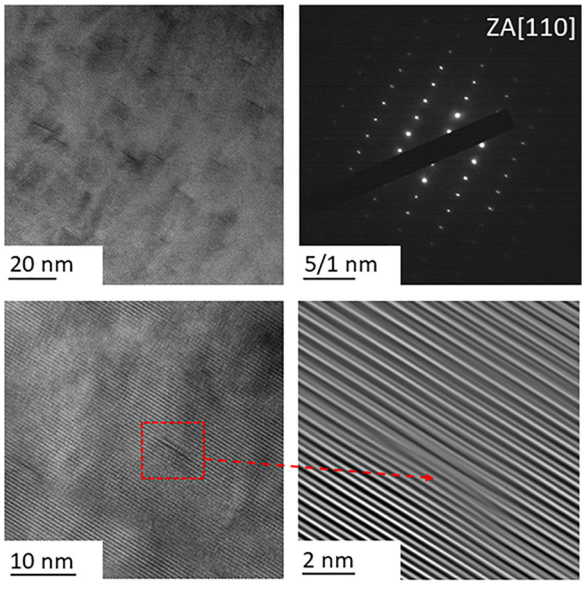

FIG. 1. Cross-sectional high resolution TEM (HRTEM) image of the uppermost region of the epi layer, showing the presence of the stacking fault (SF) (top left). Selected area diffraction pattern (top right) shows the reflection of the [110] zone axis. High magnification HRTEM image (bottom left) and corresponding inverse fast Fourier transform (IFFT) image (bottom right) showing individual defects. SF density was determined by counting the number of imaged SF in a cross-sectional TEM sample.

A full area Ti (20 nm)/Au (80 nm) backside Ohmic contact was formed by rapid thermal annealing at 550 °C under N_2 ambience. A bilayer dielectric consisting of 40 nm of Al_2O_3 and 360 nm of SiN_x was used for the field plate, after first cleaning the epi surface with UV ozone for 10 min to remove surface contamination.[43] These layers were deposited on top of the drift layer using a Cambridge-Nano-Fiji atomic layer deposition (ALD) and Plasma-Therm plasma enhanced chemical vapor deposition (PECVD) system, respectively. Field-plates with different sized windows (0.4×0.4 mm^2 to 1×1 mm^2) were opened with buffered oxide etch (BOE), and a 500 nm thick Ni (420 nm)/Au (80 nm) Schottky contact was deposited by e-beam evaporation and patterned using standard photolithography. An additional layer of SiN_x (200 nm) was deposited on the sample surface, and 21 devices with a leakage current of less than 50 μA were opened with BOE for the metal contact. This was roughly 50% of the total number of devices (44) on the sample. These devices were interconnected with an Au metal using e-beam evaporation and a gold plating process, as shown in the process schematic of Fig. 2. The total rectifying contact area of the resulting array was 0.09 cm^2. Figure 3 (top left) shows an example of a 0.4×0.4 mm^2 device (the inset shows a variety of device sizes on the mask-set, but we used only the larger 0.4×0.4 and 1×1 mm^2 rectifiers) as well as a schematic of the individual rectifiers (top right). The bottom of the figure shows optical microscopy images of the completed array taken at different magnification. The current-voltage (I-V), current density-voltage (J-V), and capacitance-voltage (C-V) characteristics were measured in air at 25–150 °C on an Agilent 4145B parameter analyzer and a 4284A Precision LCR Meter. For reverse voltages >100 V and forward currents >100 mA, a Tektronix 370A curve tracer was used due to the rating limits of the Agilent analyzer.

Figure 4 shows the forward (top) and reverse (bottom) single-sweep J-V characteristics along with the on-off ratio of a representative device on this wafer. Assuming that thermionic emission is the dominant transport mechanism, the Schottky barrier height and ideality factor of these devices are 1.01 eV and 1.01, respectively. We did not observe any enhancement due to fluorine incorporation effects, as has been reported by others.[22] The diameter dependence of the breakdown voltage showed that this was dominated by bulk contributions and not surface effects, and from limited data, we estimated a surface recombination velocity of $\leq 10^5$ cm s^{-1} on these edge terminated diodes. This indicates that the performance is not surface-related in this technology. The device on-off ratio was measured at a fixed forward current of 1 V and a reverse current of 0 to −100 V and was in the range of

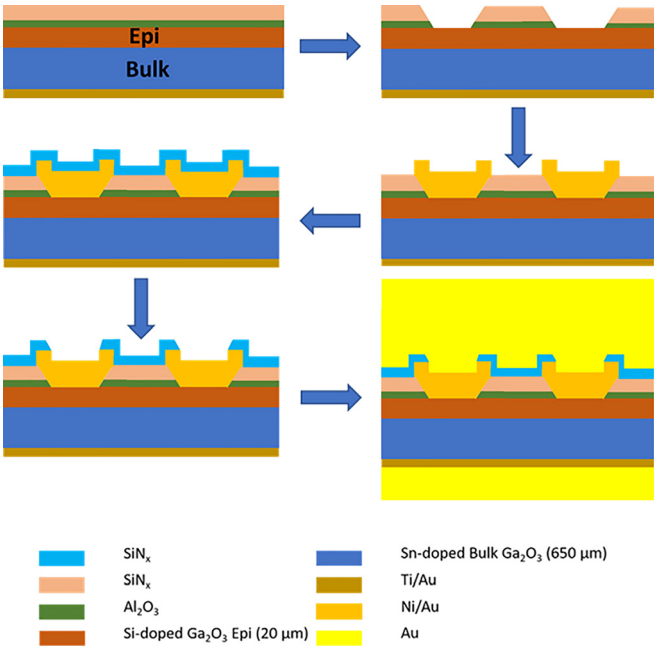

FIG. 2. Schematic of the process to fabricate rectifier arrays by interconnecting individual rectifiers.

10^6–10^8. The specific on-resistance (Ron) was ~10 m cm^2, which includes the substrate resistance component of 2.8 m cm^2. These results are consistent with those previously reported for Ni/Au Schottky contacts on Ga_2O_3.[35–41] Since these were single sweeps, excessive self-heating was not a significant issue and the devices showed no degradation in performance. It is clear that pushing the devices to high forward current under dc conditions can lead to thermal degradation characterized by epi layer delamination because of

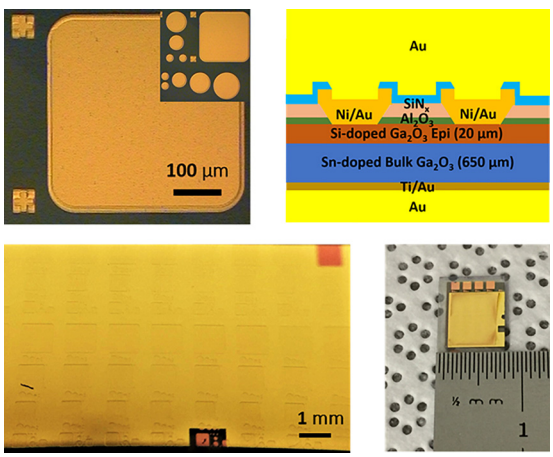

FIG. 3. Optical microscopy image of individual 0.4 × 0.4 mm^2 rectifiers (top left) showing the entire maskset in the inset, schematic of individual rectifiers with thick Au as an interconnect metal (top right), and optical microscopy images of arrays (bottom, left, and right).

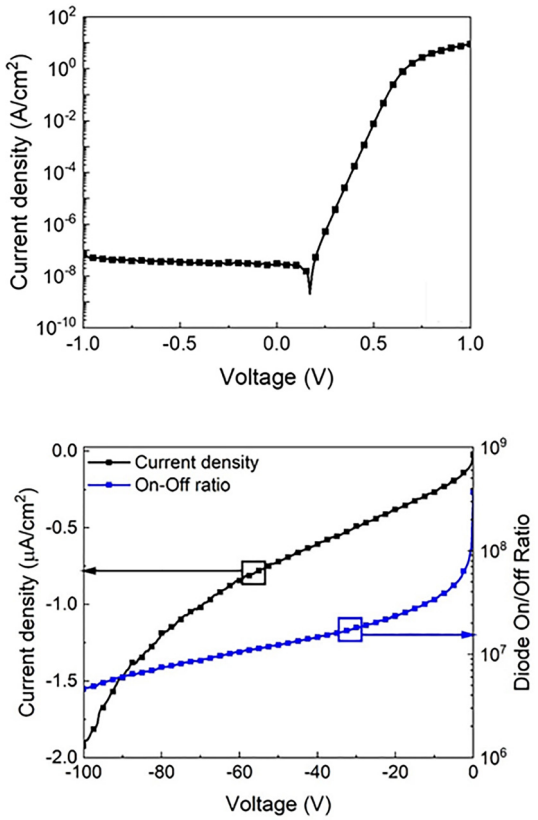

FIG. 4. Current density-voltage characteristics of individual rectifiers (top) and reverse current density and on-off ratio (bottom) for individual rectifiers with an area of 1 × 1 mm^2.

differential heating within the rectifier structure.[43] The low thermal conductivity of Ga_2O_3 means that practical devices must include packaging approaches with cooling by both topside and backside heat extraction, with the type being developed for both GaN and SiC.[15,32–34] Finally, note that the breakdown occurs in Ga_2O_3 and not in the field plate, as discussed elsewhere.[46]

To put this work in context, the drift layer doping in our rectifiers is among the lowest reported. The 2.44 kV devices reported previously had 10 μm thick epi layers with a doping of 10^{16} cm^{-3} at the surface to 2×10^{16} cm^{-3} at depths beyond 2.5 μm and breakdown of ~400 V for devices of 150 μm diameter,[8] while 1 kV devices were obtained on 7 μm drift layers with a doping of 1.8×10^{16} cm^{-3}.[22] Our drift layers are 1.62×10^{16} cm^{-3}, with a constant profile from the surface throughout the layer, exhibiting breakdown voltages from ~1 kV for 150 μm diameter devices to 240 V for an area of 1 mm^2. Our value of on-resistance of 10 m cm^2 for 1 mm^2 devices compares well with previous results in which R_{ON} reduces with the increasing area ratio of the fin-channels and was 11.3 m cm^{-2} for 2–4 μm diameter fin devices and 7 m cm^2 for 150 μm diameter devices.[8] Field-plated devices with a breakdown voltage of 1 kV had R_{ON} values of 5.1 m cm^2 for 200–400 μm diameter devices.[22] Thus, in terms of breakdown, on-resistance, and drift layer doping, the current devices are representative of the state-of-the-art.

Figure 5 shows the forward (top) and reverse (center) J-V characteristics for the 21 device array of interconnected rectifiers and its on-off ratio at a fixed forward current of 4 V (bottom). The maximum current was 33.2 A (367 A cm^{-2}), with a reverse breakdown voltage (V_B) of 240 V (defined as the voltage for a current density of 1 μA cm^{-2}). This current density demonstrates that large area interconnected structures in Ga_2O_3 can sustain the same levels achieved in small area rectifiers. Note that the breakdown voltage is roughly a factor of 20 below the theoretical maximum for this doping/thickness of the drift layer and is a result of using large area devices, in which it is more likely to have a crystal defect. The breakdown voltage was over 1 kV for small diameter (<100 μm) rectifiers, but we are aiming for high total current and small area devices do not provide large forward currents. The on-state resistance (R_{ON}) was 0.012 Ω cm^2, with a forward turn-on voltage of 2.9 V (defined at 100 A cm^{-2}). The total forward current was 10 A at 1.9 V and 22 A at 3 V. The power figure-of-merit (FOM), V_B^2/R_{ON}, was 4.8 MW cm^{-2}. The device on-off ratio is in the range of 10^5–10^{10} over the reverse voltage range of 1–100 V. The simulated maximum electric field at the contact periphery was 0.25 MV cm^{-1}, showing that there is still significant room for optimization. The individual device reverse recovery was also measured, with a reverse recovery time of 32 ns with an I_{rr} value of 55 mA. This showed no significant temperature dependence over the temperature range of 25–150 °C (activation energy <0.05 eV). Under high level injection conditions, the effective carrier lifetime τ is given by $\tau_s/[\mathrm{erf}^{-1}(1 + I_R/I_F)]$, where τ_s is the carrier storage time in the epi layer and I_R and I_F are the reverse current during storage time and the forward on-state current, respectively.[18] The recovery time of 32 ns leads to an estimated high injection carrier lifetime of ~0.1 ns. This is roughly consistent with the observed minority carrier diffusion length of ~350 nm.[47] The direct bandgap of Ga_2O_3 is advantageous in achieving rapid switching times.

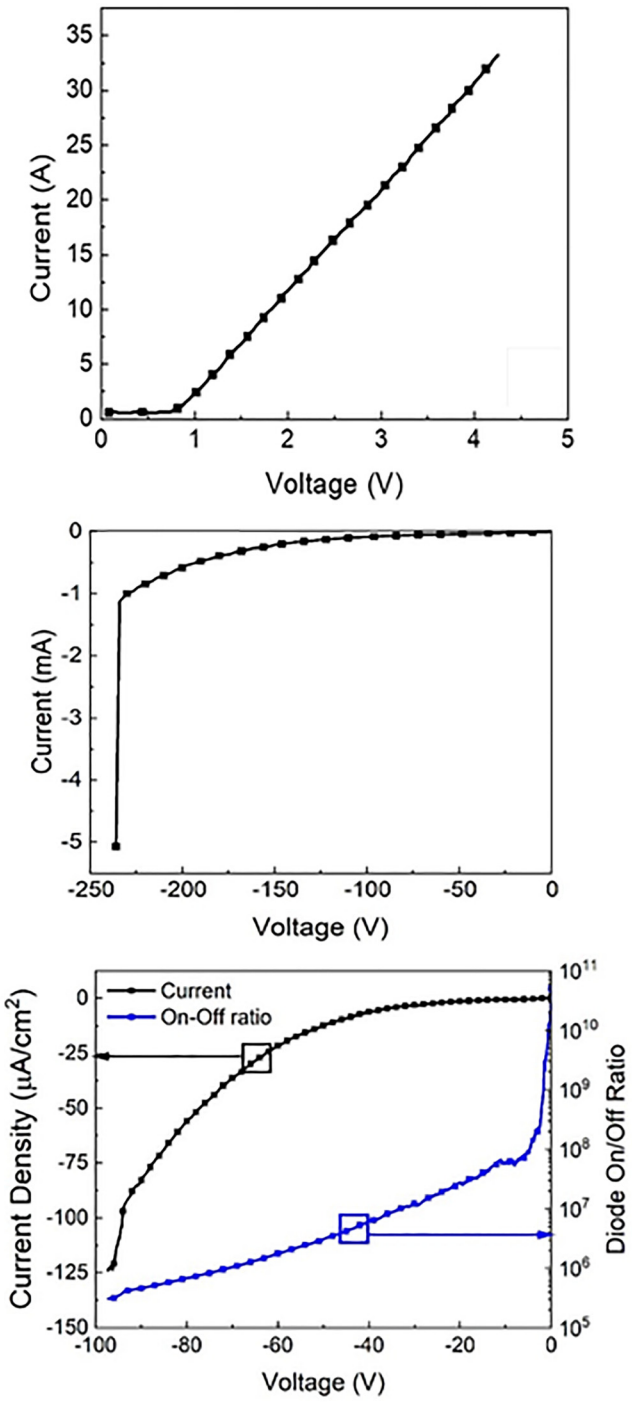

FIG. 5. Forward (top) and reverse (center) current characteristics from arrays and reverse current density and on-off ratio of arrays (bottom).

In summary, we report the demonstration of a Ga_2O_3 rectifier array capable of >30 A of forward absolute current in the single sweep mode, with a device breakdown of 240 V and low surface recombination velocity ($\leq 10^5$ cm s^{-1}). The device has an on-resistance of 0.012 Ω cm^2 and a power figure-of-merit (FOM) of 4.8 MW/cm^2, and the yield is limited by the defect density in the starting material and correlates with the observed threading screw and basal dislocation densities. These results are another milestone for Ga_2O_3 toward its path for promising high-power electronic device applications since rectifiers are needed in inverter modules of power conversion systems.

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REFERENCES

[1]M. Higashiwaki, A. Kuramata, H. Murakami, and Y. Kumagai, J. Phys. D: Appl. Phys. **50**, 333002 (2017).

[2]A. J. Green, K. D. Chabak, E. R. Heller, R. C. Fitch, M. Baldini, A. Fiedler, K. Irmscher, G. Wagner, Z. Galazka, S. E. Tetlak, A. Crespo, K. Leedy, and G. H. Jessen, IEEE Electron Device Lett. **37**, 902 (2016).
[3]M. Higashiwaki and G. H. Jessen, Appl. Phys. Lett. **112**, 060401 (2018).
[4]S. J. Pearton, J. Yang, P. Cary, F. Ren, J. Kim, M. Tadjer, and M. Mastro, Appl. Phys. Rev. **5**, 011301 (2018).
[5]Z. Galazka, Semicond. Sci. Technol. **33**, 113001 (2018).
[6]M. J. Tadjer, N. A. Mahadik, J. A. Freitas, E. R. Glaser, A. D. Koehler, L. E. Luna, B. N. Feigelson, K. D. Hobart, F. J. Kub, and A. Kuramata, Proc. SPIE **10532**, 1053212 (2018).
[7]A. Takatsuka, K. Sasaki, D. Wakimoto, Q. T. Thieu, Y. Koishikawa, J. Arima, J. Hirabayashi, D. Inokuchi, Y. Fukumitsu, A. Kuramata, and S. Yamakoshi, in 2018 76th Device Research Conference (DRC), June (2018), pp. 1–2.
[8]W. Li, Z. Hu, K. Nomoto, R. Jinno, Z. Zhang, T. Q. Tu, K. Sasaki, A. Kuramata, D. Jena, and G. H. Xing, in 2018 IEEE International Electron Devices Meeting (IEDM) (2018), p. 8.5.1.
[9]J. C. Yang, F. Ren, M. J. Tadjer, and A. Kuramata, ECS J. Solid State Sci. Technol. **7**, Q92 (2018).
[10]W. Lee, S. Li, D. Han, B. Sarlioglu, T. Minav, and M. Pietola, IEEE Trans. Transp. Electrification **4**, 684 (2018).
[11]A. Huang, Proc. IEEE **105**, 2019 (2017).
[12]F. Roccaforte, P. Fiorenza, G. Greco, R. L.Nigro, F. Giannazzo, F. Iucolano, and M. Saggio, Microelectron. Eng. **187**, 66 (2018).
[13]A. Kuramata, K. Koshi, S. Watanabe, Y. Yamaoka, T. Masui, and S. Yamakoshi, Jpn. J. Appl. Phys. Part 1 **55**, 1202A2 (2016).
[14]S. B. Reese, T. Remo, J. Green, and A. Zakutayev, "Gallium oxide power electronics: Towards silicon cost and silicon carbide performance," Joule **3**, 903 (2019).
[15]M. Tadjer, Electrochem. Soc. Interface **27**, 49–52 (2018).
[16]N. Ma, N. Tanen, A. Verma, Z. Guo, T. Luo, H. Xing, and D. Jena, Appl. Phys. Lett. **109**, 212101 (2016).
[17]See https://www.ut-ec.co.jp/english/portfolio/flosfia for "Applications of Gallium Oxide rectifiers,"; See also https://spectrum.ieee.org/semiconductors/materials/gallium-oxide-power-electronics-cool-new-flavor for "Power Electronics Applications."
[18]K. Fujihira, S. Tamura, T. Kimoto, and H. Matsunami, IEEE Trans. Electron Devices **49**, 150 (2002).
[19]J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, AIP Adv. **8**, 055026 (2018).
[20]Z. Cheng, L. Yates, J. Shi, M. J. Tadjer, K. D. Hobart, and S. Graham, APL Mater. **7**, 031118 (2019).
[21]P. Paret, G. Moreno, B. Kekelia, R. Kotecha, X. Feng, K. Bennion, B. Mather, A. Zakutayev, S. Narumanchi, S. Graham, and S. Kim, in 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), October (2018), pp 287–294.
[22]K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, Appl. Phys. Lett. **110**, 103506 (2017).
[23]B. Chatterjee, A. Jayawardena, E. Heller, D. W. Snyder, S. Dhar, and S. Choi, Rev. Sci. Instrum. **89**, 114903 (2018).
[24]Y. Zhang, A. Neal, Z. Xia, C. Joishi, J. Johnson, Y. Zheng, S. Bajaj, M. Brenner, D. Dorsey, K. Chabak, G. Jessen, J. Hwang, S. Mou, J. Heremans, and S. Rajan, Appl. Phys. Lett. **112**, 173502 (2018).
[25]E. Ahmadi, O. S. Koksaldi, X. Zheng, T. Mates, Y. Oshima, U. K. Mishra, and J. S. Speck, Appl. Phys. Express **10**, 071101 (2017).
[26]S. Krishnamoorthy, Z. Xia, C. Joishi, Y. Zhang, J. McGlone, J. Johnson, M. Brenner, A. R. Arehart, J. Hwang, and S. Lodha, Appl. Phys. Lett. **111**, 023502 (2017).
[27]S. Fujita, M. Oda, K. Kaneko, and T. Hitora, Jpn. J. Appl. Phys. Part 1 **55**, 1202A3 (2016).
[28]M. Oda, R. Tokuda, H. Kambara, T. Tanikawa, T. Sasaki, and T. Hitora, Appl. Phys. Express **9**, 021101 (2016).
[29]J. Noh, M. Si, H. Zhou, M. J. Tadjer, and P. D. Ye, in Proceedings of 2018 76th Device Research Conference (2018).
[30]K. Sasaki, D. Wakimoto, Q. T. Thieu, Y. Koishikawa, A. Kuramata, M. Higashiwaki, and S. Yamakoshi, IEEE Electron Device Lett. **38**, 783 (2017).
[31]H. Zhou, K. Maize, G. Qiu, A. Shakouri, and P. D. Ye, Appl. Phys. Lett. **111**, 092102 (2017).
[32]T. J. Anderson, K. D. Hobart, M. J. Tadjer, A. D. Koehler, T. I. Feygelson, B. B. Pate, J. K. Hite, F. J. Kub, and C. R. Eddy, ECS Trans. **64**, 185 (2014).
[33]E. Heller, S. Choi, D. Dorsey, R. Vetur, and S. Graham, Microelectron. Reliab. **53**, 872 (2013).
[34]H. Zhang, S. S. Ang, H. A. Mantooth, and S. Krishnamurthy, "A high temperature, double-sided cooling SiC power electronics module," in 2013 IEEE Energy Conversion Congress and Exposition (2013), pp. 2877–2883.
[35]Q. He, W. Mu, H. Dong, S. Long, Z. Jia, H. Lv, Q. Liu, M. Tang, X. Tao, and M. Liu, Appl. Phys. Lett. **110**, 093503 (2017).
[36]J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, J. Kim, and A. Kuramata, Appl. Phys. Lett. **110**, 192101 (2017).
[37]J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, and A. Kuramata, IEEE Electron Dev. Lett. **38**, 906 (2017).
[38]G. Jian, Q. He, W. Mu, B. Fu, H. Dong, Y. Qin, Y. Zhang, H. Xue, S. Lon, and Z. Jia, AIP Adv. **8**, 015316 (2018).
[39]J. Yang, F. Ren, Y. T. Chen, Y. T. Liao, C. W. Chang, J. Lin, M. J. Tadjer, S. J. Pearton, and A. Kuramata, IEEE J. Electron Devices Soc. **7**, 57 (2019).
[40]C.-H. Lin, N. Hatta, K. Konishi, S. Watanabe, A. Kuramata, K. Yagi, and M. Higashiwaki, Appl. Phys. Lett. **114**, 032103 (2019).
[41]Q. He, W. Mu, B. Fu, Z. Jia, S. Long, Z. Yu, Z. Yao, W. Wang, H. Dong, Y. Qin, G. Jian, Y. Zhang, H. Xue, H. Lv, Q. Liu, M. T. X. Tao, and M. Liu, IEEE Electron Device Lett. **39**, 556 (2018).
[42]J. Yang, F. Ren, S. J. Pearton, and A. Kuramata, IEEE Trans. Electron Devices **65**, 2790 (2018).
[43]J. Yang, C. Fares, F. Ren, Y. T. Chen, Y. T. Liao, C. W. Chang, J. Lin, M. Tadjer, D. J. Smith, S. J. Pearton, and A. Kuramata, ECS J. Solid State Sci. Technol. **8**, Q3028 (2019).
[44]N. A. Mahadik, M. J. Tadjer, P. L. Bonanno, K. D. Hobart, R. E. Stahlbush, T. J. Anderson, and A. Kuramata, APL Mater. **7**, 022513 (2019).
[45]S. Masuya, K. Sasaki, A. Kuramata, S. Yamakoshi, O. Ueda, and M. Kasu, Jpn. J. Appl. Phys. Part 1 **58**, 055501 (2019).
[46]P. H. Carey IV, J. Yang, F. Ren, R. Sharma, M. Law, and S. J. Pearton, ECS J. Solid State Sci. Technol. **8**, Q3221 (2019).
[47]E. B. Yakimov, A. Y. Polyakov, N. B. Smirnov, I. V. Shchemerov, J. Yang, F. Ren, G. Yang, J. Kim, and S. J. Pearton, J. Appl. Phys. **123**, 185704 (2018).